TDC1147

Monolithic Video A/D Converter

7-Bit, 15 Msps

Features

- 20 Msps conversion rate
- No digital pipeline delay
- 7-bit resolution
- 1/2 LSB linearity
- Sample-and-hold circuit not required
- TTL compatible
- Selectable output format
- Availabb in 24 pin CERDIP

Applications

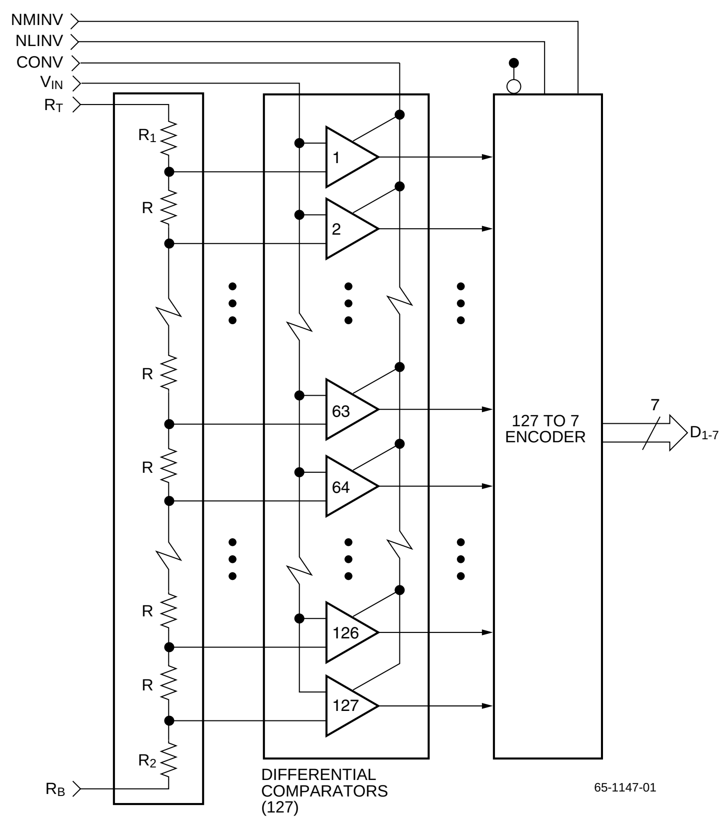
- Low-cost video digitizing
- Medical imaging
- Data acquisition
- High resolution A/D converters
- Telecommunications systems
- Radar data conversion

Description

The TDC1147 is a 7-bit flash analog-to-digital converter which has no pipeline delay between sampling and valid data. The output data register normally found on flash A/D converters has been bypassed allowing data to transfer directly to output drivers from the encoding logic section of the circuit. The converter requires only one clock pulse to perform the complete conversion operation. The conversion time is guaranteed to be less than 60 nanoseconds.

The TDC1147 is function and pin-compatible with Raytheon's TDC1047 7-bit flash A/D converter which has an output data register. The TDC1147 will operate accurately at sampling rates up to 15 Msps and has an analog bandwidth of 7 MHz. Linearity errors are guaranteed to be less than 0.4% over the operating temperature range.

Block Diagram



Functional Description

General Information

The TDC1147 has two functional sections: a comparator array and encoding logic. The comparator array compares the input signal with 127 reference voltages to produce an N-of-127 code (sometimes referred to as a "thermometer" code, as all the comparators referred to voltages more positive than the input signal will be off, and those referred to voltages more negative than the input signal will be on). The encoding logic converts the N-of-127 code into binary or offset two's complement coding, and can invert either output code. This coding function is controlled by DC signals on pins NMINV and NLINV.

Power

The TDC1147 operates from two supply voltages, +5.0V and -5.2V. The return path for I_{CC} (the current drawn from the +5.0V supply) is D_{GND}. The return path for I_{EE} (the current drawn from the -5.2V supply) is A_{GND}. All power and ground pins must be connected.

Reference

The TDC1147 converts analog signals in the range $V_{RB} \le V_{IN} \le V_{RT}$ into digital form. V_{RB} (the voltage applied to the pin at the bottom of the reference resistor chain) and V_{RT} (the voltage applied to the pin at the top of the reference resistor chain) should be between +0.1V and -1.1V. V_{RT} should be more positive than V_{RB} within that range. The voltage applied across the reference resistor chain (V_{RT}-V_{RB}) must be between 0.8V and 1.2V. The nominal voltages are V_{RT} = 0.00V and V_{RB} = -1.00V. These voltages may be varied dynamically up to 7MHz. Due to slight variations in the reference current with clock and input signals, R_T and R_B should be low-impedance points. For circuits in which the reference is not varied, a bypass capacitor to ground is recommended. If the reference inputs are varied dynamically as in an Automatic Gain Control (AGC) circuit, a low-impedance reference source is recommended.

Controls

Two function control pins, NMINV and NLINV are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the Output Coding Table.

Convert

The TDC1147 uses a CONVert (CONV) input signal to initiate the A/D conversion process. Unlike other flash A/D converters which have a one-clock-cycle pipeline delay between sampling and output data, the TDC1147 requires only a single pulse to perform the entire conversion operation. The analog input is sampled (comparators are latched) within the maximum Sampling Time Offset (t_{STO}, see Figure 1). Data from that sample becomes valid after a maximum Output Delay Time (t_D) while data from the previous sample is held at the outputs for a minimum Output Hold Time (t_{HO}). This allows data from the TDC1147 to be acquired by an external register or other circuitry. Note that there are minimum time requirements for the HIGH and LOW portions (t_{PWH}, t_{PWL}) of the CONV waveform and all output timing specifications are measured with respect to the rising edge of CONV.

Analog Input

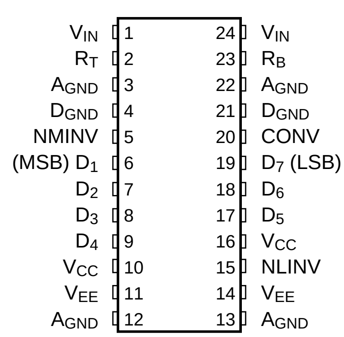
The TDC1147 uses latching comparators which cause the input impedance to vary slightly with the signal level. For optimal performance, both V_{IN} pins must be used and the source impedance of the driving circuit must be less than 30 Ohms. The input signal will not damage the TDC1147 if it remains within the range of V_{EE} to +0.5V. If the input signal is between the V_{RT} and V_{RB} references, the output will be a binary number between 0 and 127 inclusive. A signal outside this range will indicate either full-scale positive or full-scale negative, depending on whether the signal is off-scale in the positive or negative direction.

Outputs

The outputs of the TDC1147 are TTL compatible, and capable of driving four low-power Schottky TTL (54/74 LS) unit loads. The outputs hold the previous data a minimum time (t_{HO}) after the rising edge of the CONV signal. New data becomes valid after a maximum time (t_D) after the rising edge of the CONV signal. The use of 2.2 KΩ pull-up resistors is recommended.

Pin Assignments

24 Lead Ceramic DIP



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Pin Definitions

Pin Name	Pin Number	Value	Pin Function Description
Power			
V_{CC}	10, 16	+5.0V	Positive Supply Voltage
V_{EE}	11, 14	-5.2V	Negative Supply Voltage
D_{GND}	4, 21	0.0V	Digital Ground
A_{GND}	3, 12, 13, 22	0.0V	Analog Ground
Reference			
R_T	2	0.00V	Reference Resistor (Top)
R_B	23	-1.00V	Reference Resistor (Bottom)
Controls			
NMINV	5	TTL	Not Most Significant Bit INVert
NLINV	15	TTL	Not Least Significant Bit INVert
Convert			
CONV	20	TTL	Convert
Analog Input			
V_{IN}	1, 24	0V to -1V	Analog Signal Input
Outputs			
D_1	6	TTL	MSB Output
D_2–D_6	7–9, 17, 18	TTL	
D_7	19	TTL	LSB Output

Absolute Maximum Ratings (beyond which the device will be damaged)[1]

Parameter		Min.	Max.	Unit
Supply Voltages				
V_{CC} (measured to D_{GND})		-0.5	+7.0	V
V_{EE} (measured to A_{GND})		-7.0	+0.5	V
A_{GND} (measured to D_{GND})		-0.5	+0.5	V
Input Voltages				
CONV, NMINV, NLINV (measured to D_{GND})		-0.5	+5.5	V
V_{IN}, V_{RT}, V_{RB} (measured to A_{GND})		+0.5	V_{EE}	V
V_{RT} (measured to V_{RB})		-2.2	+2.2	V
Output				
Applied voltage (measured to D_{GND})[2]		-0.5	5.5	V
Applied current, externally forced[3,4]		-1.0	6.0	mA
Short circuit duration (single output in high state to ground)			1	sec
Temperature				
Operating	Case	-55	+125	°C
	Junction		+175	°C
Lead, soldering (10 seconds)			+300	°C
Storage		-65	+150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

Operating Conditions

Parameters		Temperature Range						Units
		Standard			Extended			
		Min.	Nom.	Max.	Min.	Nom.	Max.	
V_{CC}	Positive Supply Voltage (measured to D_{GND})	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{EE}	Negative Supply Voltage (measured to A_{GND})	-4.9	-5.2	-5.5	-4.9	-5.2	-5.5	V
V_{AGND}	Analog Ground Voltage (measured to D_{GND})	-0.1	0.0	0.1	-0.1	0.0	0.1	V
t_{PWL}	CONV Pulse Width, (LOW)	22			22			ns
t_{PWH}	CONV Pulse Width, (HIGH)	18			18			ns
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			2.0	mA
I_{OH}	Output Current, Logic HIGH			-0.4			-0.4	mA
V_{RT}	Most Positive Reference Input[1]	-0.1	0.0	0.1	-0.1	0.0	0.1	V
V_{RB}	Most Negative Reference Inputs[1]	-0.9	-1.0	-1.1	-0.9	-1.0	-1.1	V
V_{RT}-V_{RB}	Voltage Reference Differential	0.8	1.0	1.2	0.8	1.0	1.2	V
V_{IN}	Input Voltage	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V

Operating Conditions (continued)

Parameters		Temperature Range						Units
		Standard			Extended			
		Min.	Nom.	Max.	Min.	Nom.	Max.	
T_A	Ambient Temperature, Still Air	0		70				
T_C	Case Temperature				-55		125	°C

Note:
1. V_{RT} must be more positive than V_{RB}, and voltage reference differential must be within specfied range.

DC Electrical Characteristics

Parameter		Test Conditions		Temperature Range				Units
				Standard		Extended		
				Min.	Max.	Min.	Max.	
I_{CC}	Positive Supply Current	V_{CC} = Max, static[1]			25		30	mA
I_{EE}	Negative Supply Current	V_{EE} = Max, static[1]						
		T_A = 0°C to 70°C			-170			mA
		T_A = 70°C			-135			mA
		T_C = -55°C to 125°C					-220	mA
		T_C = 125°C					-130	mA
I_{REF}	Reference Current	V_{RT}, V_{RB} = Nom			35		50	mA
R_{REF}	Total Reference Resistance			34		20		Ω
R_{IN}	Input Equivalent Resistance	V_{RT}, V_{RB} = Nom, V_{IN} = V_{RB}		100		40		KΩ
C_{IN}	Input Capacitance				60		60	pF
I_{CB}	Input Constant Bias Current	V_{EE} = Max			160		300	µA
I_{IL}	Input Current, Logic LOW	V_{CC} = Max, V_I = 0.5V	CONV		-0.4		-0.6	mA
			NMINV, NLINV		-0.6		-0.8	mA
I_{IH}	Input Current, Logic HIGH	V_{CC} = Max, V_I = 2.4V			50		50	µA
I_I	Input Current, Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1.0		1.0	mA
V_{OL}	Output Voltage, Logic LOW	V_{CC} = Min, I_{OL} = Max			0.5		0.5	V
V_{OH}	Output Voltage, Logic HIGH	V_{CC} = Min, I_{OH} = Max		2.4		2.4		V
I_{OS}	Short Circuit Output Current	V_{CC} = MAX, one pin to ground, one second duration.			-30		-30	mA
C_I	Digital Input Capacitance	T_A = 25°C, F = 1MHz			15		15	pF

Note:
1. Worst case, all digital inputs and outputs LOW.

AC Electrical Characteristics

Parameter		Test Conditions	Temperature Range Standard Min.	Standard Max.	Extended Min.	Extended Max.	Units
F_S	Maximum Conversion Rate	V_{CC} = Min, V_{EE} = Min	15		15		MSPS
t_{STO}	Sampling Time Offset	V_{CC} = Min, V_{EE} = Min		7		10	ns
t_D	Output Delay	V_{CC} = Min, V_{EE} = Min, Load 1		60		70	ns
t_{HO}	Output Hold Time	V_{CC} = MAX, V_{EE} = Max, Load 1	15		15		ns

Timing Diagram

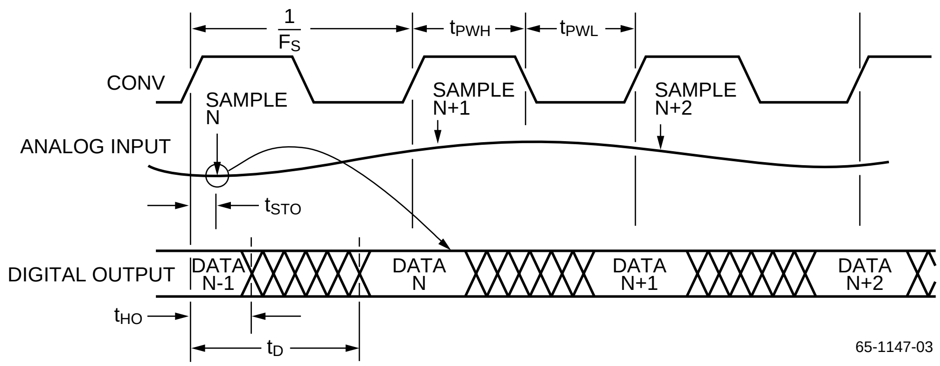


Figure 1. Timing Diagram

System Performance Characteristics

Parameter		Test Conditions	Temperature Range Standard Min.	Standard Max.	Extended Min.	Extended Max.	Units
E_{LI}	Linearity Error, Integral Independent	V_{RT}, V_{RB} = Nom		0.4		0.4	%
E_{LD}	Linearity Error, Differential			0.4		0.4	%
C_S	Code Size	V_{RT}, V_{RB} = Nom	30	170	30	170	% Nominal
V_{OT}	Offset Voltage, Top	V_{IN} = V_{RT}		+50		+50	mV
E_{OB}	Offset Voltage, Bottom	V_{IN} = V_{RB}		-30		-30	mV
T_{CO}	Temperature Coefficient			±20		±20	µV/°C
BW	Bandwidth, Full Power Input		7		7		MHz
t_{TR}	Transient Response, Full-Scale			10		10	ns
SNR	Signal-to-Noise Ratio	7MHz Bandwidth, 20MSPS Conversion					
	Peak Signal/RMS Noise	1 MHz Input	45		46		dB
		7 MHz Input	43		44		dB
	RMS Signal/RMS Noise	1 MHz Input	36		37		dB
		7 MHz Input	34		35		dB
E_{AP}	Aperture Error			50		50	ps
DP	Differential Phase Error[1]	F_S = 4 x NTSC		1.5		1.5	Degree
DG	Differential Gain Error[1]	F_S = 4 x NTSC		2.5		2.5	%

Note:

1. In Excess of quantization.

Equivalent Circuits

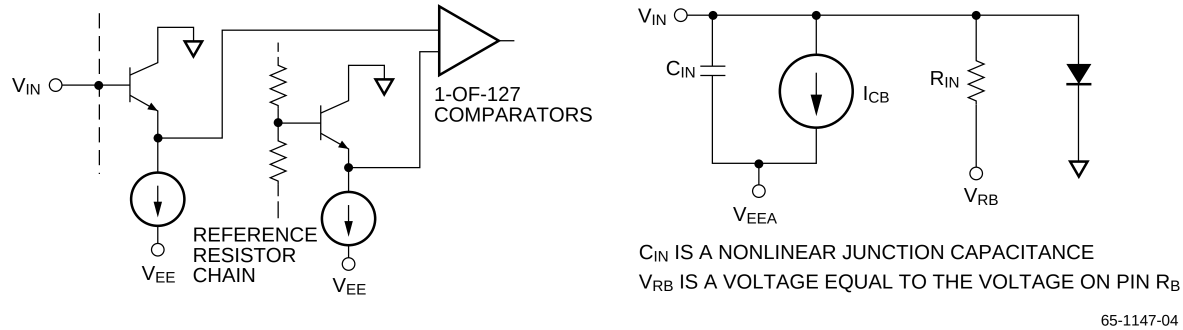


Figure 2. Simplified Analog Input Equivalent Circuit

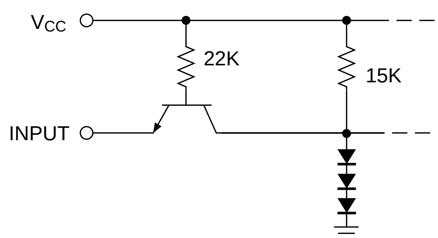


Figure 3. Digital Input Equivalent Circuit

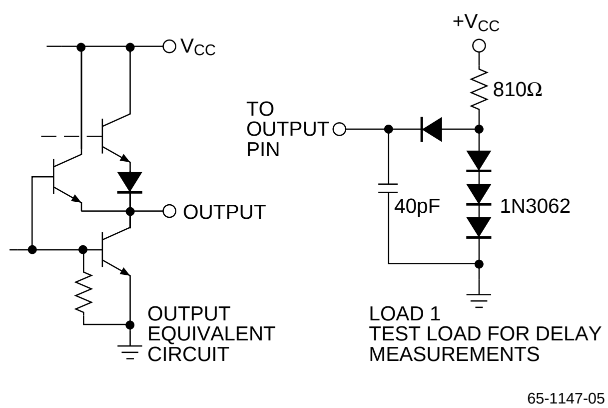


Figure 4. Output Circuits

Output Coding Table

	Binary		Offset Two's Complement	
Range	**True**	**Inverted**	**True**	**Inverted**
-1.00V FS	**NMINV = 1** **NLINV = 1**	**0** **0**	**0** **1**	**1** **0**
0.0000V	0000000	1111111	1000000	0111111
–0.0078V	0000001	1111110	1000001	0111110
• • •	• • •	• • •	• • •	• • •
–0.4960V	0111111	1000000	1111111	0000000
–0.5039V	1000000	0111111	0000000	1111111
• • •	• • •	• • •	• • •	• • •
–0.9921V	1111110	0000001	0111110	1000001
–1.0000V	1111111	0000000	0111111	1000000

Note:

1. Voltages are code midpoints.

Applications Discussion

Calibration

To calibrate the TDC1147, adjust V_{RT} and V_{RB} to set the 1st and 127th thresholds to the desired voltages. Assuming a 0V to -1V input range, continuously strobe the converter with -0.0039V (1/2 LSB from 0V) on the analog input, and adjust V_{RT} for output toggling between codes 00 and 01. Then apply -0.996V (1/2 LSB from -1V) and adjust V_{RB} for toggling between codes 126 and 127.

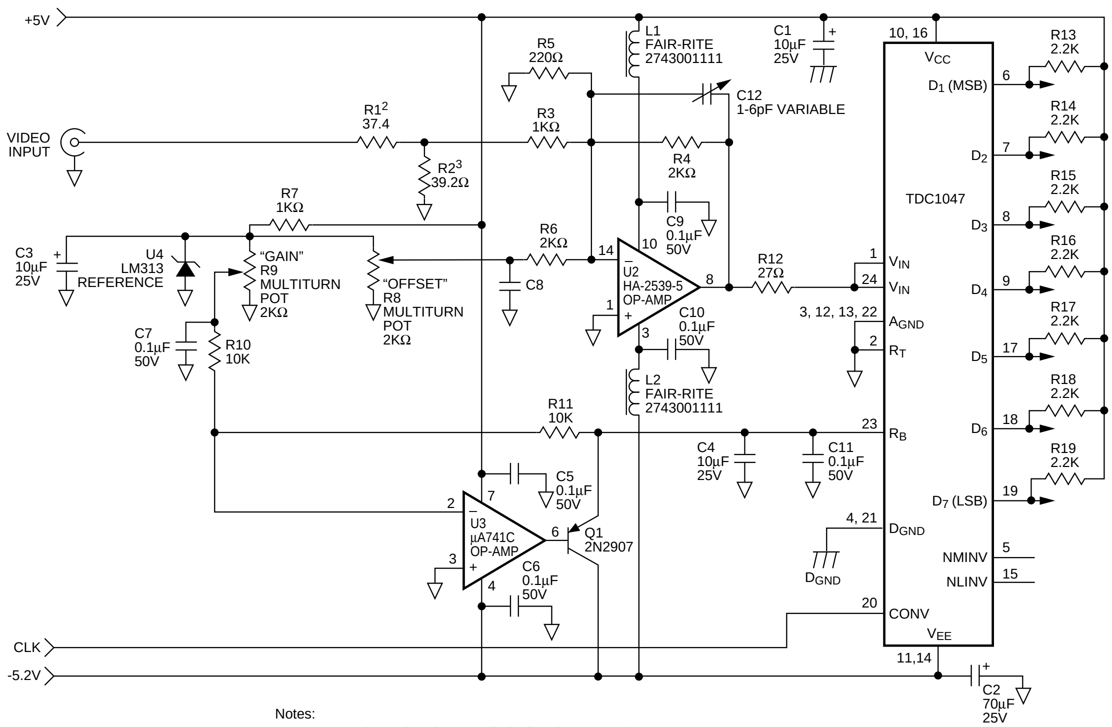
The degree of required adjustment is indicated by the offset voltages, V_{OT} and V_{OB}. Offset voltages are generated by the inherent parasitic resistance between the package pin and the actual resistor chain on the integrated circuit. These parasitic resistors are shown as R_1 and R_2 in the Block Diagram. Calibration will cancel all offset voltages, eliminating offset and gain errors.

The above method for calibration requires that both ends of the resistor chain, R_T and R_B are driven by variable voltage sources. Instead of adjusting V_{RT}, R_T can be connected to analog ground and the 0V end of the range calibrated with an input amplifier offset control. The offset error at the bottom of the resistor chain causes a slight gain error, which can be compensated for by varying the voltage applied to R_B. The bottom reference is a convenient point for gain adjust that is not in the analog signal path.

Typical Interface Circuit

Figure 5 shows an example of a typical interface circuit for the TDC1147. The analog input amplifier is a bipolar wide-band operational amplifier, which is used to directly drive the A/D converter. Bipolar inputs may be accommodated by adjusting the offset control. A zener diode provides a stable reference for both the offset and gain control. The amplifier has a gain of -1 providing the recommended 1Vp-p input for the A/D converter. Proper decoupling is recommended for all supplies, although the degree of decoupling shown may not be needed. A variable capacitor permits either step response or frequency response optimization. This may be replaced with a fixed capacitor, whose value depends upon the circuit board layout and desired optimization.

The bottom reference voltage, V_{RB}, is supplied by an inverting amplifier, followed with a PNP transistor. The transistor provides a low-impedance source and is necessary to sink the current flowing through the reference resistor chain. The bottom reference voltage can be adjusted to cancel the gain error introduced by the offset voltage, V_{OB}, as discussed in the Calibration section.



Notes:

1. Unless otherwise specified, all resistors are 1/4W, 2%.
2. $R1 = Z_{IN} - \left(\frac{1000\ R2}{1000 + R2}\right)$
3. $R2 = \frac{1}{\left(\frac{2V_{Range}}{V_{REF}\ Z_{IN}}\right) - 0.001}$

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Figure 5. Typical Interface Circuit

Notes:

Notes:

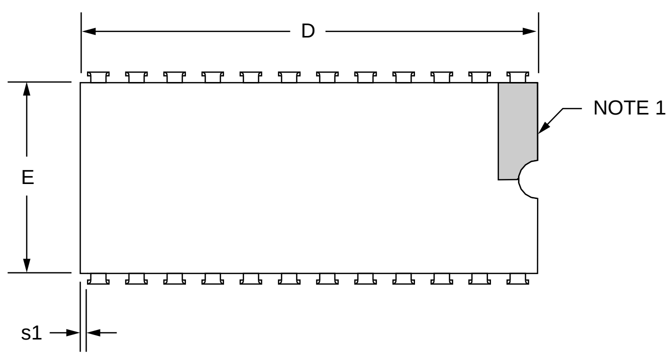
Mechanical Dimensions

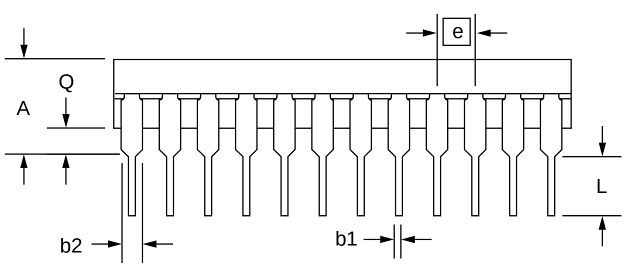
24 Lead Ceramic DIP

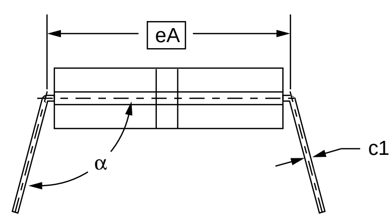
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.225	—	5.72	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	—	1.290	—	32.77	4
E	.500	.610	12.70	15.49	4
e	.100 BSC		2.54 BSC		5, 9
eA	.600 BSC		15.24 BSC		7
L	.120	.200	3.05	5.08	
Q	.015	.075	.38	1.91	3
s1	.005	—	.13	—	6
α	90°	105°	90°	105°	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 12, 13 and 24 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus and glass overrun.
5. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 24.
6. Applies to all four corners (leads number 1, 12, 13, and 24).
7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "α" is 90°.
8. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
9. Twenty-two spaces.







Ordering Information

Product Number	Temperature Range	Screening	Package	PackageMarking
TDC1147B7C	STD–T_A = 0°C to 70°C	Commercial	24 Lead Ceramic DIP	1147B7C
TDC1147B7V	EXT–T_C = -55°C to 125°C	MIL-STD-883	24 Lead Ceramic DIP	1147B7V

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